

(19) 日本国特許庁 (J P)

(12) 公開特許公報 (A)

(11)特許出願公開番号
特開2001-298157
(P2001-298157A)

(43)公開日 平成13年10月26日(2001.10.26)

(51) Int.Cl.⁷
H 0 1 L 27/04
21/822

識別記号

F I
H01L 27/04

テ-71-ト⁺ (参考)

(21)出願番号 特願2000-113065(P2000-113065)

(71) 出願人 000004237

日本電気株式会社

東京都港区芝五丁目7番1号

(22) 出願日 平成12年4月14日(2000.4.14)

(72) 発明者 堀 良彦

東京都港区芝五丁目7番1号 日本電気株式会社内

(72) 発明者 村田 俊一

東京都港区芝五丁目7番1号 日本電気株式会社内

(74) 代理人 100082935

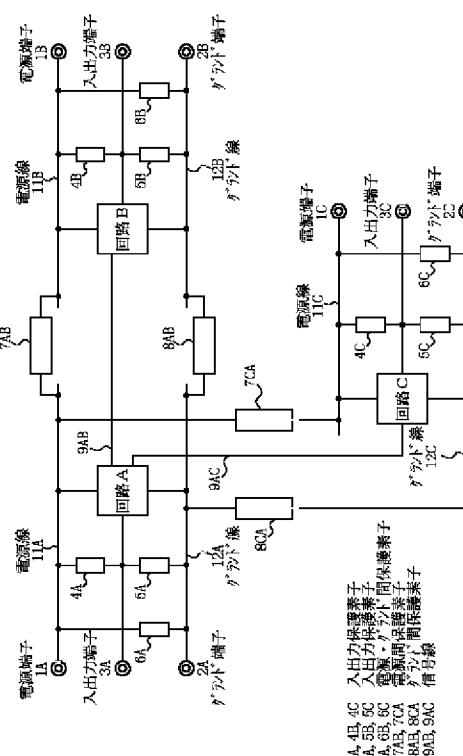
弁理士 京本 直樹 (外2名)
Fターム(参考) 5F038 BE09 BH04 BH05 BH07 BH13
BH15 CA07 CD02 CD05 EZ20

(54) 【発明の名称】 保護回路及びこれを搭載した半導体集積回路

(57) 【要約】

【課題】電源電力の供給路を各回路毎に独立させた複数の回路を組み合せて所望の信号処理を行う構成の回路を、少ない数の保護素子で、外来の異常高電圧から確実に保護することができる。

【解決手段】外部から電源電力を受け取るための独立した電源端子及びグランド端子の対（1Aと2A, 1Bと2B, 1Cと2C）と、電源端子とグランド端子との間に設けられた電源・グランド間保護素子6A, 6B, 6Cとを少なくとも有する複数の回路A, B, Cの内、回路間が信号線9AB, 9ACで結ばれている回路の組合せ（回路AとB及び回路AとC）に限って、電源端子どうし（端子1Aと1B及び端子1Aと1C）の間に及び、グランド端子どうし（端子2Aと2B及び端子2Aと2C）の間に電源間保護素子7AB, 7CA及びグランド間保護素子8AB, 8CAを設ける。



【特許請求の範囲】

【請求項1】 外部から電源電力を受け取るための独立した高位電源端子及び低位電源端子の対と、前記高位電源端子と低位電源端子との間に設けられて、所定の値以上の電圧が加わったときインピーダンスが低下して前記高位電源端子と低位電源端子とを低インピーダンスで接続する高位・低位電源間保護素子とを少なくとも有する複数の回路に対し、回路間の高位電源端子どうしの間及び低位電源端子どうしの間に、所定の値以上の電圧が加わったときインピーダンスが低下して、前記高位電源端子どうしの間又は前記低位電源端子どうしの間を低インピーダンスで接続する高位電源間保護素子及び低位電源間保護素子を設けた保護回路において、

前記複数の回路に、回路間が信号線で結ばれていない回路の組合せが有るとき、前記高位電源間保護素子及び低位電源間保護素子を、回路間が信号線で結ばれている回路の組合せに限って、設けたことを特徴とする保護回路。

【請求項2】 前記信号線で結ばれている回路の内少なくとも1つ以上は外部と信号をやり取りするための外部端子を有し、

前記外部との信号授受のための外部端子を有する回路は、前記信号授受のための外部端子と高位電源端子との間又は低位電源端子との間の少なくとも一方に、所定の値以上の電圧が加わったときインピーダンスが低下して、前記信号授受のための外部端子と高位電源端子との間又は低位電源端子との間を低インピーダンスで接続する入出力保護素子を備えることを特徴とする、請求項1に記載の保護回路。

【請求項3】 同一チップ上に、外部から電源電力を受け取るための独立した高位電源端子及び低位電源端子の対と、前記高位電源端子と低位電源端子との間に設けられて、所定の値以上の電圧が加わったときインピーダンスが低下して前記高位電源端子と低位電源端子とを低インピーダンスで接続する高位・低位電源間保護素子とを少なくとも有する複数の回路と、回路間の高位電源端子どうしの間又は低位電源端子どうしの間に設けられて、所定の値以上の電圧が加わったときインピーダンスが低下して、前記高位電源端子どうしの間又は前記低位電源端子どうしの間を低インピーダンスで接続する高位電源間保護素子及び低位電源間保護素子を備える半導体集積回路において、

前記複数の回路に、回路間が信号線で結ばれていない回路の組合せが有るとき、前記高位電源間保護素子及び低位電源間保護素子を、回路間が信号線で結ばれている回路の組合せに限って、設けたことを特徴とする半導体集積回路。

【請求項4】 前記信号線で結ばれている回路の内少なくとも1つ以上は外部と信号をやり取りするための外部端子を有し、

前記外部との信号授受のための外部端子を有する回路は、前記信号授受のための外部端子と高位電源端子との間又は低位電源端子との間の少なくとも一方に、所定の値以上の電圧が加わったときインピーダンスが低下して、前記外部端子と高位電源端子との間又は低位電源端子との間を低インピーダンスで接続する入出力保護素子を備えることを特徴とする、請求項3に記載の半導体集積回路。

【請求項5】 前記高位・低位電源間保護素子、高位電源間保護素子、低位電源間保護素子及び入出力保護素子に、p-n接合ダイオードを用いたことを特徴とする、請求項1若しくは請求項2に記載の保護回路又は、請求項3若しくは請求項4に記載の半導体集積回路。

【請求項6】 前記高位・低位電源間保護素子、高位電源間保護素子、低位電源間保護素子及び入出力保護素子に、流路電極の一方と制御電極とを接続してダイオード接続としたMOS電界効果トランジスタを用いたことを特徴とする、請求項1若しくは請求項2に記載の保護回路又は、請求項3若しくは請求項4に記載の半導体集積回路。

【請求項7】 前記信号線で結ばれた回路の組合せの内の少なくとも1組は、互いの回路の電源電圧が異なっていることを特徴とする、請求項3乃至6のいずれかに記載の半導体集積回路。

【発明の詳細な説明】**【0001】**

【発明の属する技術分野】 本発明は、保護回路及びこれを搭載した半導体集積回路に関し、特に、それぞれ異なる独立の電源電力供給路を持つ複数の回路を組み合せて所望の信号処理を実行する構成の回路を、静電気のような外来の異常高電圧から保護する回路と、そのような保護回路を搭載した半導体集積回路に関する。

【0002】

【従来の技術】 この種の保護回路について、半導体集積回路(LSI)を例にとって、説明する。図6は、従来の技術による保護回路を搭載したLSIの、回路ブロックの配置の一例を示す。図6を参照して、このLSIは、回路A、回路B、回路Cの3つの回路を備えている。回路Aと回路Bとが回路間の信号線9ABで結ばれている。また回路Aと回路Cとが、回路間の信号線9ACで接続されている。回路Bと回路Cとの間には、回路間の信号線はない。各回路A、B、Cはそれぞれ、例えばCMOS構成のインバータやNANDゲート或いはNORゲートなどを含んでいて、回路Aと回路Bとの間の信号線9ABは、回路Aの信号出力点(pMOSトランジスタとnMOSトランジスタのドレイン電極どうしの接続点)と、回路Bの信号入力点(pMOSトランジスタとnMOSトランジスタの共通のゲート電極)とを接続している。回路Aと回路Cの組合せについても、同じである。

【0003】各回路A, B, Cは、それぞれ毎に独立して外部から電源電力を受け取るために、外部電源端子と外部グランド端子の組（1Aと2A, 1Bと2B, 1Cと2C）を1組ずつ備えている。また外部と信号を取りするために、入出力端子3A, 3B, 3Cを備えている。更に、回路Aは、電源端子1Aと入出力端子3Aとの間に入出力保護素子4Aを備え、グランド端子2Aと入出力端子3Aとの間に入出力保護素子5Aを有し、電源端子1Aとグランド端子2Aとの間には電源・グランド間保護素子6Aが設けられている。同様に、回路Bは保護素子4B, 5B, 6Bを備え、回路Cは保護素子4C, 5C, 6Cを有している。各保護素子は、例えば回路Aの場合であれば、外部端子である電源端子1A、グランド端子2A或いは入出力端子3Aに静電気のような外来の異常高電圧が印加されたとき、その異常高電圧が回路A内の例えば上記MOSトランジスタのような回路素子に直接加わるのを防いで、回路を保護するためのものである。

【0004】上述の入出力保護素子及び電源・グランド間保護素子は、端子間に或る一定電圧が掛るまでは絶縁状態であり、それ以上の電圧が加わると導通状態になる特性を示す素子であって、導通状態に変化するときの端子間電圧が回路A, B, C内の保護すべき回路素子の耐圧以下であること、導通時のインピーダンスが低いこと、電圧が印加されてから導通するまでの時間が短いことなどの条件を満たすことが求められる。保護素子としては、上記の条件を満足するものであればどのような構造のものであってもよいが、半導体集積回路にあっては、製造プロセスの整合性などの点から、p-n接合ダイオードや、ゲート電極とドレイン（又は、ソース）電極とを結んでダイオード接続にしたMOSトランジスタの順方向電圧や逆方向の降伏電圧を利用することが多く、図7に数例を示すような、p-n接合ダイオードやダイオード接続のMOSトランジスタを単独で、或いは複数個を組み合せて保護素子としたものを、図8に一例を示すように、各回路A, B, Cの外部電源端子、外部入出力端子、外部グランド端子の間に接続する。

【0005】ここで、この図6に示されるLSIは、3つの回路A, B, Cが外部や互いの回路どうしの間で信号を取りながら、LSI全体として所望の信号処理を行うわけであるが、本発明との関連でいえば、回路Aと回路Bとは信号線9ABで結ばれ、回路Aと回路Cとは信号線9ACで結ばれて、互いに信号を取りするのに対し、回路Bと回路Cとの間では信号の授受がない点、つまり、全ての回路どうしが信号線で結ばれているわけではない点に一つの特徴がある。また各回路A, B, Cが、外部から電源電力の供給を受けるための外部電源端子及び外部グランド端子の組を、互いに独立に備えている点にもう一つの特徴がある。本発明は、上述の二つの特徴を備えた回路を、静電気のような外来の異常

電圧から保護する技術に関わるものである。

【0006】上述の第二の特徴は、以下のような理由による。すなわち、一般にLSIは、同一チップ上に形成されたいくつかの独立した回路（以下、小回路と記す。図6中の回路A, B, Cに相当する）が信号線で結ばれて、外部とチップとの間或いは小回路どうしの間で信号を取りながら所望の信号処理を行うものであって、当然、各小回路には動作に必要な電源電力が供給されなければならない。この小回路に対する電源電力の供給は、最も単純には、チップ上に外部から電源電力を受け取るための高位電源端子と低位電源端子の対を1対だけ設け、その1対の外部電源端子からチップ上の全ての小回路に電源線を走らすことによって、実現できる。しかしながら、近年、LSIが大規模化し、高機能化、高性能化するのに伴い、上述のような、1対の外部電源端子だけでチップ上の全ての小回路に電源電力を供給する構造では、LSIが目的とする信号処理に支障が生じるようになってきている。

【0007】一例として、電源線を共通にしている場合には、その電源線に生じたノイズ性の電源電圧の変動（高位電源電位の低下、または低位電源電位の上昇）が、電源線を通じて各小回路の動作不安定にさせたり、場合によっては誤動作を起こさせることがある。上記のノイズ性の電源電圧の変動は、例えば出力バッファのような動作電流の大きい回路が、複数、外部の回路と信号を取りながら動作するために一齊にスイッチ動作をするなどのように、各小回路の動作に伴って電源線に一時的に大きな動作電流が流れたときに、電源線の配線抵抗によって電源電位VCCが低下したり或いはグランド電位が浮き上がりたりすることによって生じる。このような現象が発生したときに、例えば各1本ずつの高位電源線と低位電源線とでLSI内の全ての小回路に電源電力を供給しているものとすると、或る幾つかの小回路が同時に動作することで、別的小回路の電源電位VCCやグランド電位も大きく変化することとなる。その結果、その別的小回路では、そこで扱う信号の振幅に対して動作マージンが小さくなったり、誤動作を起こし易くなったり、或いは出力信号の振幅が小さくなったり、次段の小回路が誤動作し易くなる。更には、ノイズの程度によっては、ノイズだけで小回路の状態が反転してしまうことにもなりかねない。そこで、或る小回路と他の小回路とで高位電源線も低位電源線も別々にすることで、或る小回路が動作することによるノイズ性の電源電圧の変動が、高位電源線や低位電源線を通して他の小回路を動作不安定にしたり誤動作させるのを遮断するのである。

【0008】再び図6を参照して、この図に示すLSIは、各回路A, B, C毎に入出力保護素子4Aと5A, 4Bと5B, 4Cと5Cを備え、また電源・グランド間保護素子6A, 6B, 6Cを有している。従って、各回路毎では、いずれの外部端子の間に静電気のような異常

高電圧が印加されても、それによる電荷は各回路の保護素子を通って各回路の電源線或いはグランド線に放電され、静電気のエネルギーの大部分は保護素子により消費されて、回路の内部の素子は破壊から免れる。例えば、回路Aにおいて、入出力端子3Aとグランド端子2Aとの間に静電気が印加されたものとする。この場合、静電気による電荷は、入出力保護素子5Aを通ってグランド線12Aに流れ、回路A内の素子に静電気が加わることはない。同様に、入出力端子3Aと電源端子1Aとの間に静電気が加わったときは、電荷が入出力保護素子4Aを通って電源線11Aに流れることによって、回路Aが保護される。また電源端子1Aとグランド端子2Aとの間に静電気が加わった場合は、回路Aは電源・グランド間保護素子6Aによって保護される。このように、回路Aに対して、外部電源端子1A、外部グランド端子2Aまたは入出力端子3Aのいずれに外来の異常高電圧が加わっても、回路Aは保護素子4A, 5A, 6Aによって保護される。同じことが、他2つの回路B、回路Cについてもいえる。

【0009】しかしながら、LSI全体で考えた場合、或る回路の外部端子とこれとは別の回路の外部端子との間に異常高電圧が加わった場合には、保護機能が作用せず、回路が破壊されることがある。以下に、その説明をする。図8に、例えば回路Aの外部端子と回路Bの外部端子との間に静電気が加わった状態を示す。尚、以下の説明において、この場合の回路Cは保護動作には特には関与しないので、図8は、これを簡略にして理解を容易にするために、回路Cの部分を省いて示す。図8を参照して、回路Aの入出力端子3Aと回路Bのグランド端子2Bとの間に、入出力端子3Aの方が正となるような静電気が加わったものとする。このとき、静電気による電荷は、図8中に矢印の付いた実線で示すように、回路Aの入出力保護素子4Aを通って、一旦は回路Aの電源線11Aに流れ。ところが、その電源線11Aはそれから先、回路B側のどの配線にも接続していないので、電源線11Aに流れた電荷は回路Aの内部に逆流し、回路A内にあって回路Bへ信号を出力する素子10ABから信号線9ABを通り、更に、回路B内にあって回路Aから信号を受け取る素子10BAを通って、回路Bのグランド線12Bに抜ける。その結果、回路A内及び回路B内にあって信号線9ABを介して信号をやり取りする素子10ABと素子10BAとが破壊されてしまうことになる。

【0010】上述のような、各回路A, B, C毎に電源電力の供給路が独立していることが原因で生じる回路の破壊は、回路間の電源線どうしの間及びグランド線どうしの間に保護素子を挿入することによって防ぐことができる。図9に、各回路間の電源線どうし、グランド線どうしの間に保護素子を設けた構造のLSIの回路ブロックの配置図を示す。図9を参照して、この図に示すLSI

は、回路Aの電源線11Aと回路Bの電源線11Bとの間、回路Bの電源線11Bと回路Cの電源線11Cとの間及び回路Cの電源線11Cと回路Aの電源線11Aとの間に、それぞれ電源間保護素子7AB, 7BC, 7CAが接続されている。また回路Aのグランド線12Aと回路Bのグランド線12Bとの間、回路Bのグランド線12Bと回路Cのグランド線12Cとの間及び回路Cのグランド線12Cと回路Aのグランド線12Aとの間に、それぞれグランド間保護素子8AB, 8BC, 8CAを備えている。電源間保護素子7AB, 7BC, 7CA及びグランド間保護素子8AB, 8BC, 8CAのそれぞれには、例えば図7(b)に示すような構造のものが用いられる。この構造の保護素子は、両方の回路の電源電圧が等しい場合に多く用いられる。またどちらか一方の電源電圧が低い場合は、図7(a)に示す構造のものが用いられる。更には、まれにではあるが、保護素子の両端における電圧変動が大きく、図7(a)や図7(b)の構造では通常状態でも導通してしまう場合は、図7(c)や図7(d)に示す構造のものを用いることもある。

【0011】いずれにしろ、図9に示す構造のLSIにおいて、前述したと同様に、回路Aの入出力端子3Aと回路Bのグランド端子2Bとの間に、入出力端子3Aの方が正になるような静電気が加わったものとすると、これによる電荷は、図9中に矢印の付いた実線で示すように、回路Aの入出力保護素子4Aから電源線11Aに流れ、更に、回路Aの電源線と回路Bの電源線との間に設けた電源間保護素子7ABを通って、回路Bの電源・グランド間保護素子6Bからグランド線12Bに抜ける。或いは、矢印の付いた破線で示すように、回路Aの入出力保護素子5Aからグランド線12Aに流れ、更に、回路Aのグランド線と回路Bのグランド線との間に設けたグランド間保護素子8ABを通って、回路Bのグランド線12Bに抜ける。どちらの放電経路を通るかは、保護素子や配線のインピーダンス或いは保護素子が導通状態に変化する電圧などによって決る。上に述べたのは、回路Aの入出力端子3Aと回路Bのグランド端子2Bとの間に異常高電圧が加わった例であるが、3つの回路A, B, Cどうしの間で、各外部端子1A, 2A, 3A, 1B, 2B, 3B, 1C, 2C, 3Cのどの組合せの間に高電圧が加わった場合でも、またいずれの放電経路を辿った場合でも、静電気による電荷が回路Aや回路Bの内部に流れ込むことはなく、各回路A, B, Cは確実に保護される。

【0012】

【発明が解決しようとする課題】上述したように、チップ上の各小回路がそれぞれ毎に外部から独立して電源電力の供給を受ける構造のLSIの場合でも、図9に示すように、各小回路どうしの間で、電源線と電源線との間及びグランド線とグランド線との間に、それぞれ電源間保護素子又はグランド間保護素子を設けることによっ

て、異なる小回路の外部端子間に外来の異常高電圧が印加されたときでも、各小回路を破壊から保護できる。

【0013】しかしながら、図9に示すように、全ての小回路の組合せに対して電源間保護素子とグランド間保護素子とを設けると、小回路の数、換言すれば独立した電源電力の供給路の数が多くなると、それにつれて電源間保護素子及びグランド間保護素子の数が非常に多くなってしまうという問題が生じる。すなわち、小回路の数をn個（但し、nは2以上）とすると、電源間保護素子とグランド間保護素子の組の数は $nC_2 = n(n-1)/2$ で表される数となり、小回路の数が3個であれば、保護素子の組は、図9に示すように、3組で済むものの、小回路数が5個ならば10組、6個ならば15組といった具合に、電源間保護素子及びグランド間保護素子の組の数は、小回路の数の増加に伴ってどんどん増えて行ってしまうことになる。

【0014】従って本発明は、電源電力の供給路を各回路毎に独立させた複数の回路を組み合せて所望の信号処理を行う構成の回路を、少ない数の保護素子で、外来の異常高電圧から確実に保護できるようにすることを目的とするものである。

【0015】

【課題を解決するための手段】本発明の保護回路は、外部から電源電力を受け取るための独立した高位電源端子及び低位電源端子の対と、前記高位電源端子と低位電源端子との間に設けられて、所定の値以上の電圧が加わったときインピーダンスが低下して前記高位電源端子と低位電源端子とを低インピーダンスで接続する高位・低位電源間保護素子とを少なくとも有する複数の回路に対し、回路間の高位電源端子どうしの間及び低位電源端子どうしの間に、所定の値以上の電圧が加わったときインピーダンスが低下して、前記高位電源端子どうしの間又は前記低位電源端子どうしの間を低インピーダンスで接続する高位電源間保護素子及び低位電源間保護素子を設けた保護回路において、前記複数の回路に、回路間が信号線で結ばれていない回路の組合せが有るとき、前記高位電源間保護素子及び低位電源間保護素子を、回路間が信号線で結ばれている回路の組合せに限って、設けたことを特徴とする。

【0016】また、本発明の半導体集積回路は、同一チップ上に、外部から電源電力を受け取るための独立した高位電源端子及び低位電源端子の対と、前記高位電源端子と低位電源端子との間に設けられて、所定の値以上の電圧が加わったときインピーダンスが低下して前記高位電源端子と低位電源端子とを低インピーダンスで接続する高位・低位電源間保護素子とを少なくとも有する複数の回路と、回路間の高位電源端子どうしの間又は低位電源端子どうしの間に設けられて、所定の値以上の電圧が加わったときインピーダンスが低下して、前記高位電源端子どうしの間又は前記低位電源端子どうしの間を低

インピーダンスで接続する高位電源間保護素子及び低位電源間保護素子を備える半導体集積回路において、前記複数の回路に、回路間が信号線で結ばれていない回路の組合せが有るとき、前記高位電源間保護素子及び低位電源間保護素子を、回路間が信号線で結ばれている回路の組合せに限って、設けたことを特徴とする。

【0017】

【発明の実施の形態】次に、本発明の実施の形態について、図面を参照して説明する。図1は、本発明の一実施の形態に係る半導体集積回路の、回路ブロックの配置の一例を示す図である。図1と図9とを比較すると、本実施の形態に係るLSIは、電源間保護素子を、回路Aの電源線11Aと回路Bの電源線11Bとの間及び、回路Aの電源線11Aと回路Cの電源線11Cとの間に限って設けている点と、グランド間保護素子を、回路Aのグランド線12Aと回路Bのグランド線12Bとの間及び、回路Aのグランド線12Aと回路Cのグランド線12Cとの間だけに接続している点が、従来の技術によるLSIと異なっている。つまり、図1に示すLSIは、電源間保護素子とグランド間保護素子とを、信号線で結ばれている回路どうし（回路Aと回路B及び、回路Aと回路C）の間だけに設けていることになる。

【0018】図2に、入出力保護素子、電源間保護素子及びグランド間保護素子にpn接合ダイオードを用いた第1の実施例の、回路ブロックの配置図を示す。また、図2に示すLSIにおいて、回路Aの入出力端子3Aと回路Bのグランド端子2Bとの間に、入出力端子3Aの方が正となるような静電気が加わったときの状態を、図3に示す。尚、以下の説明において、この場合の回路Cは保護動作には特に関与しないので、図3は、これを簡略にして理解を容易にするために、回路Cの部分を省いて示す。図3を参照して、回路Aの入出力端子3Aに印加された静電気による電荷は、図3中に矢印をつけた実線で示すように、回路Aのグランド線側の入出力保護素子5Aからグランド線12Aに流れ、更に、回路Aのグランド線と回路Bのグランド線との間に設けたグランド間保護素子8ABを通って、回路Bのグランド線12Bに抜ける。或いは、矢印の付いた破線で示すように、回路Aの電源線側の入出力保護素子4Aから電源線11Aに流れ、更に、回路Aの電源線と回路Bの電源線との間に設けた電源間保護素子7ABを通って、回路Bの電源・グランド間保護素子6Bからグランド線12Bに抜ける。どのような放電経路を通るかは、保護素子や配線のインピーダンス或いは保護素子が導通状態に変化する電圧などによって決るが、いずれの放電経路を辿った場合でも、静電気による電荷は回路間の電源間保護素子7AB又はグランド間保護素子8ABを流れ、回路Aや回路Bの内部に流れ込むことはないので、回路A、Bは共に確実に保護される。

【0019】次に、静電気が加わる場合の他の例とし

て、図4に、回路Bの入出力端子3Bと回路Cの入出力端子3Cとの間に、入出力端子3Cの方が正となるような静電気が加わった状態を示す。図4を参照して、この場合は、回路Cの入出力端子3Cに印加された静電気による電荷は、図4中に矢印の付いた実線で示すように、回路Cの入出力保護素子4Cを通って電源線11Cに流れ、更に、回路Cの電源線11Cと回路Aの電源線11Aとの間に設けられた電源間保護素子7CAを通って電源線11Aに流れる。次いで、回路Aの電源線11Aと回路Cの電源線11Bとの間に設けられた電源間保護素子7BAを通って、回路Bの電源線11Bに流れ、最終的に、回路Bの入出力保護素子4Bを通って、回路Cの入出力端子3Bに流れる。或いは、矢印の付いた破線で示すように、回路Cの入出力保護素子5C→グランド線12C→回路Cのグランド線12Cと回路Aのグランド線12Aとの間のグランド間保護素子8CA→グランド線12A→回路Aのグランド線12Aと回路Bのグランド線12Bとの間のグランド間保護素子8AB→回路Bのグランド線12B→回路Bの入出力保護素子5B→回路Cの入出力端子3Bの経路で流れる。いずれの放電経路を通る場合でも、静電気による電荷が回路Aや回路Bの内部に流れ込むことはなく、各回路A, B, Cは確実に保護される。

【0020】既に述べたように、電源端子とグランド端子とを各回路毎に独立させ、電源電力供給路を異ならせたLSIで、特に静電気で破壊されやすいところは、各回路間を結ぶ信号線に接続する回路素子である。これは、図6に示すような、回路間の電源端子どうしの間及びグランド端子どうしの間に保護素子が何も挿入されていない構造のLSIにあっては、外部端子に加わった静電気は、各回路毎には、回路の電源線或いはグランド線に分散されて、各回路内の素子を破壊することはないものの、静電気が異なる回路ににまたがる場合には、その静電気による電荷が回路間の信号線を通って一方の回路から他方の回路へ流れることになり、結果として、その信号線に接続する回路素子が破壊されるからである。

【0021】これに対して、本発明によれば、各回路A, B, Cの間で、信号線で結ばれた回路どうしの電源線間及びグランド線間に保護素子を挿入することにより、LSIの外部から印加された静電気は、異なる回路の外部端子どうしの間にわたる場合でも、電源線間の保護素子7AB, 7CAやグランド線間の保護素子8AB, 8CAを通って流れるので、回路Aや回路B或いは回路Cの内部を通ることはなく、各回路A, B, Cが静電気によって破壊されることはない。

【0022】しかも本発明の場合、異なる回路の間の電源間保護素子及びグランド間保護素子は、互いに信号線で結ばれている回路どうしの間に限って設けるようにしているので、電源間保護素子及びグランド保護素子の組は、チップ内の各回路を結ぶ信号線の数だけで済むこと

になる。通常、幾つかの回路を組み合わせて更に大きな回路を作る場合でも、すべての小回路どうしが信号線で結ばれていることは少なかつたり、また各小回路は信号の処理経路に従って直列に接続されることが多いので、大抵の場合、電源間保護素子とグランド間保護素子の組は、小回路の数程度で済むことになる。例えば、図5に回路ブロックの配置図を示す第2の実施例における回路A, B, C, Dのように全ての小回路が完全に直列に接続されている場合の電源間保護素子とグランド間保護素子の組は、(小回路の数-1)組で済む。

【0023】尚、本実施の形態においては、それぞれの回路A, B, Cは全て、外部と信号をやり取りするための(外部)入出力端子3A, 3B, 3Cを備えているものとしたが、必ずしも全ての回路が外部に接続する入出力端子を持っていなくても、本発明の作用効果が損なわれることはない。また本実施の形態では、信号の入・出力用の外部端子3A, 3B, 3Cとして、1つの端子で入力用と出力用とに切り替えて用いる構造の入出力端子を用いた例について説明したが、この端子は、入力専用の端子或いは出力専用の端子であっても構わない。外部端子としての入出力端子又は入力端子若しくは出力端子を備えていない場合は、図5に示す第2の実施例のLSIのように、各回路A, B, C, Dには、敢えて入出力保護素子を設けなくてもよい。

【0024】また、図2に示す第1の実施例では、電源間保護素子7AB, 7BC, 7CA及びグランド間保護素子8AB, 8BC, 8CAに、全て同じ構造のものを用いた例を示したが、本発明はこれに限られるものではない。LSIには、例えばディジタル回路とアナログ回路とを混在させたもののような、各回路A, B, Cで電源電圧が異なるものがある。そのようなときは、電源間保護素子やグランド間保護素子として、各回路A, B, Cの電源電圧に応じて、図7に示される幾つかの保護素子から構造の異なるものを適宜選択して、組み合わせることができる。例えば、図1において、回路Aの電源電圧と回路Bの電源電圧とが同じで、回路Cの電源電圧がそれより高い場合は、回路A, B間の電源間保護素子7ABとグランド間保護素子8ABには図7(b)に示す構造のものを用い、回路A, C間の電源間保護素子7CAとグランド間保護素子8CAには図7(a)に示す構造の保護素子を用いて、ダイオードのアノードを回路A側にし、カソードを回路C側にすればよい。入出力端子保護素子4A, 5A, 4B, 5B, 4C, 5Cについても、同様に、入出力信号の振幅の関係から、それぞれ異なる構造のものを用いても構わない。

【0025】更には、電源・グランド間保護素子6A, 6B, 6Cが設けられていさえすれば、電源端子と入出力端子との間の保護素子4A, 4B, 4Cとグランド端子と入出力端子との間の保護素子5A, 5B, 5Cとは必ずしも対になつてゐなくてよく、どちらか一方だけ

でも構わない。どちらか片方を省いた場合は、導通したときのインピーダンスが十分低くなるように、残りの片方の保護素子の電流能力を倍にするのが好ましい。また、電源間保護素子7ABとグランド間保護素子8AB、電源間保護素子7CAとグランド間保護素子8CAも必ずしも対で設ける必要はなく、どちらか一方だけでもよい。しかしながら、どちらか一方だけにする場合は、上述したように、残りの方の電流能力を大きくする必要があり、保護素子の専有面積上の利点は少ないので、実用上は、放電経路の多様性を確保するという観点から、本実施の形態のように、入出力保護素子も電源間保護素子及びグランド間保護素子も、対で設けることが望ましいであろう。

【0026】なお又、これまで半導体集積回路を例にして説明したが、複数の小回路の組合せによって所望の信号処理を実行する構成の回路において、或る小回路の動作に伴うノイズ性の電源電圧の変動が、共通の電源線を介して他の小回路の状態や動作に悪影響を及ぼす現象と、電源電力の供給路を小回路毎又は幾つかの小回路のまとまり毎に独立させることによって電源電圧の変動が伝播するのを遮断するという対策については、「LSI」を「電子装置」に、「チップ」を「筐体」に読み替えれば、一般に、電子装置に対しても本発明を適用できることは明らかであろう。

【0027】

【発明の効果】以上説明したように、本発明によれば、電源電力の供給路を各回路毎に独立させた複数の回路を組み合せて所望の信号処理を行う構成の回路を、少ない数の保護素子で、外来の異常高電圧から確実に保護することができる。

【図面の簡単な説明】

【図1】本発明の一実施の形態に係る半導体集積回路の、回路ブロックの配置の一例を示す図である。

【図2】第1の実施例に係るLSIの、回路ブロックの配置を示す図である。

【図3】第1の実施例において、回路Aの入出力端子と回路Bのグランド端子との間に静電気が加わったときの状態を示す図である。

【図4】第1の実施例において、回路Cの入出力端子と回路Bの入出力端子との間に静電気が加わったときの状態を示す図である。

【図5】第2の実施例に係るLSIの、回路ブロックの配置図を示す図である。

【図6】従来の技術による一例のLSIの、回路ブロックの配置を示す図である。

【図7】保護素子の構造のいくつかの例を示す図である。

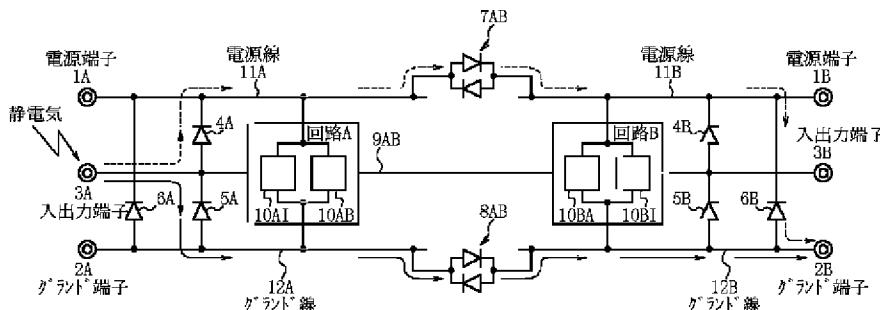
【図8】図6に示すLSIにおいて、回路Aの入出力端子と回路Bのグランド端子との間に静電気が加わったときの状態を示す図である。

【図9】従来の技術による他の例のLSIの回路ブロックの配置及び、回路Aの入出力端子と回路Bのグランド端子との間に静電気が加わったときの状態を示す図である。

【符号の説明】

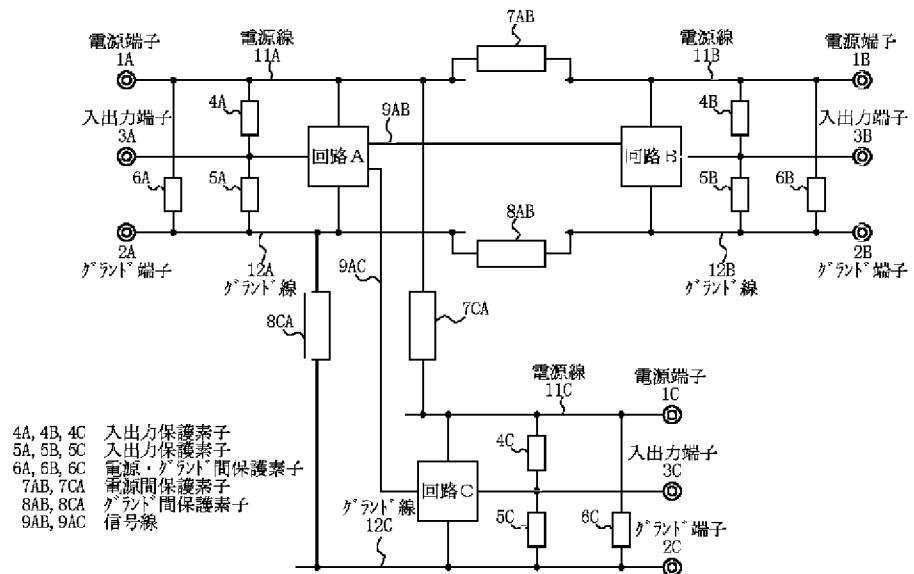
1A, 1B, 1C	電源端子
2A, 2B, 2C	グランド端子
3A, 3B, 3C	入出力端子
4A, 4B, 4C	入出力保護素子
5A, 5B, 5C	入出力保護素子
6A, 6B, 6C	電源・グランド間保護素子
7AB, 7BC, 7CA	電源間保護素子
8AB, 8BC, 8CA	グランド間保護素子
9AB, 9AC	信号線
11A, 11B, 11C	電源線
12A, 12B, 12C	グランド線

【図3】

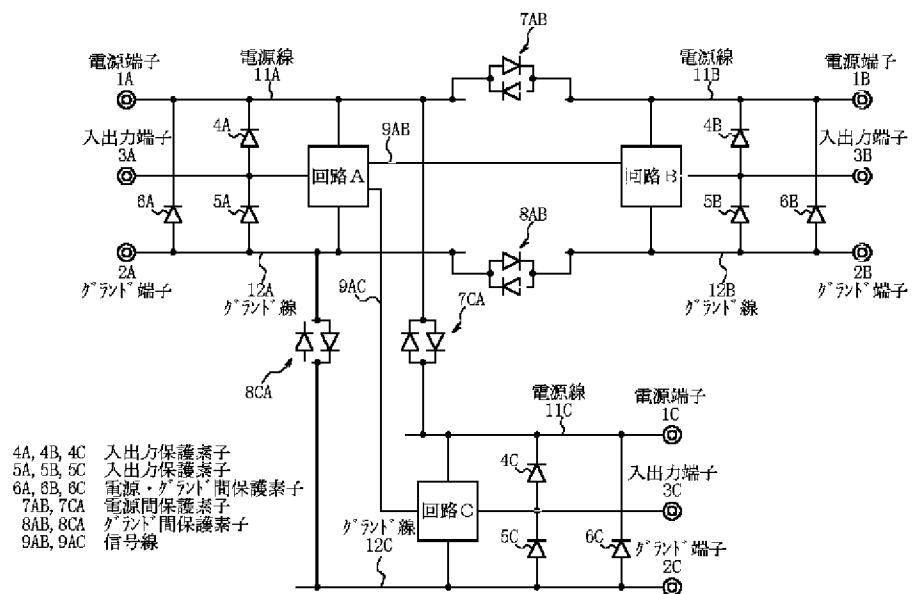


4A, 4B 入出力保護素子
5A, 5B 入出力保護素子
6A, 6B 電源・グランド間保護素子
7AB 電源間保護素子
8AB グランド間保護素子
9AB 信号線

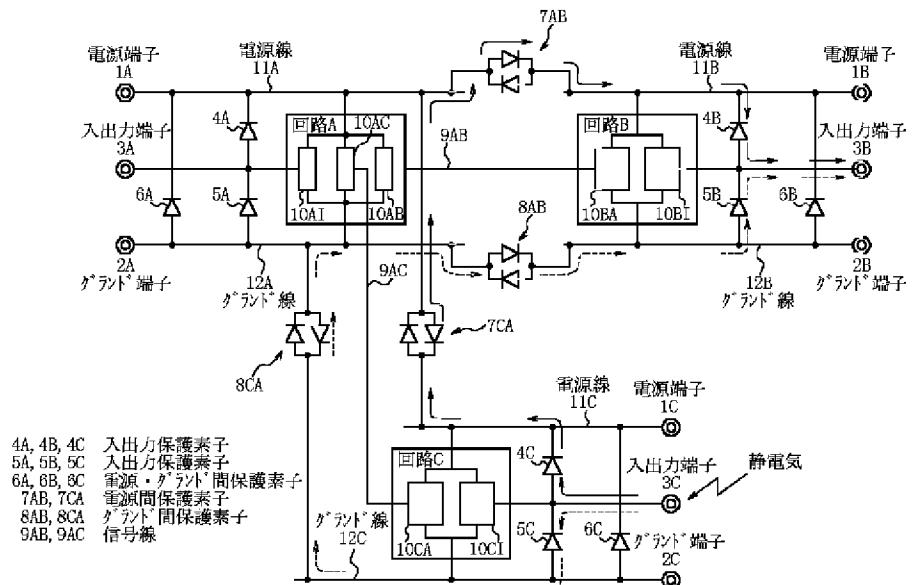
【図1】



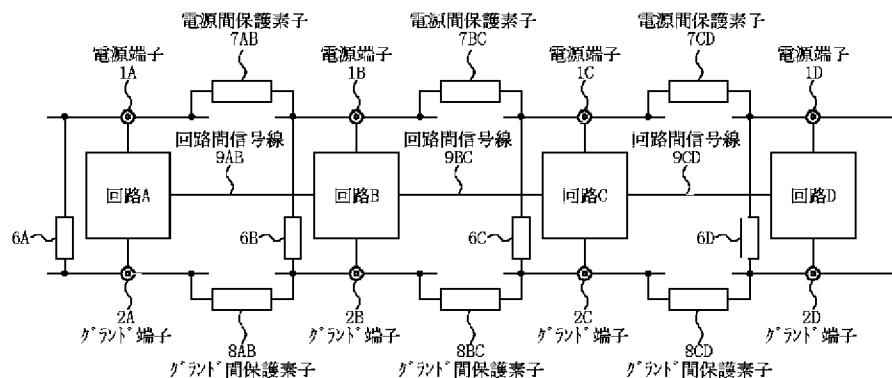
【図2】



【図4】

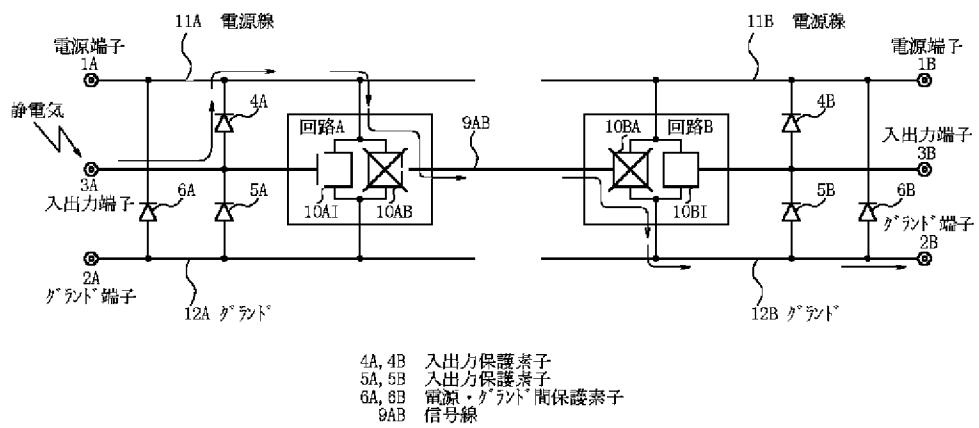


【図5】

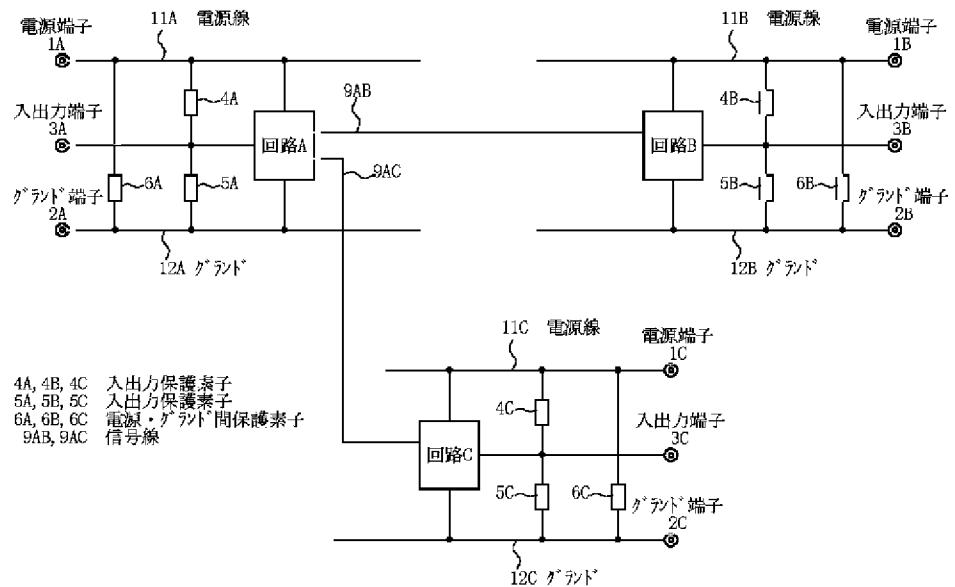


6A, 6B, 6C, 6D 電源・グランド間保護素子

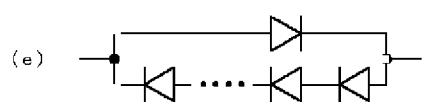
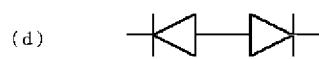
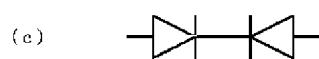
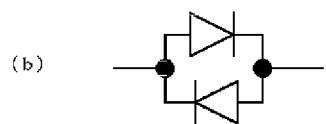
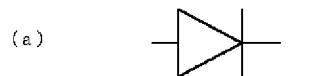
【図8】



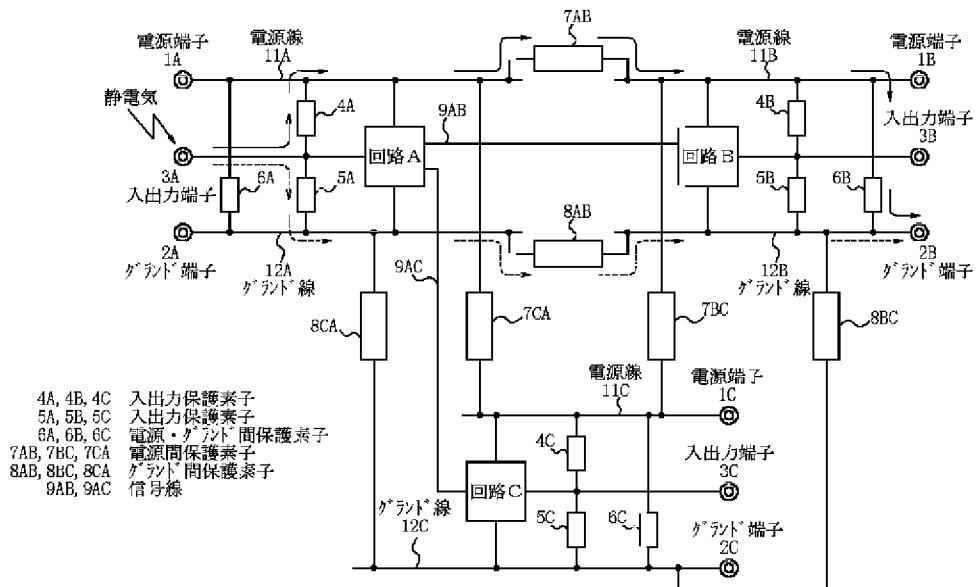
【図6】



【図7】



【図9】



PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-298157

(43)Date of publication of application : 26.10.2001

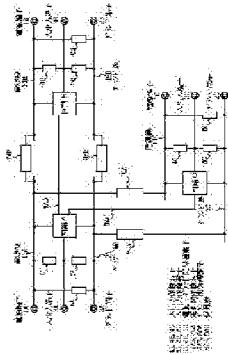
(51)Int.Cl. H01L 27/04

H01L 21/822

(21)Application number : 2000-113065 (71)Applicant : NEC CORP

(22)Date of filing : 14.04.2000 (72)Inventor : Hori Yoshihiko
Murata Shunichi

(54) PROTECTION CIRCUIT AND SEMICONDUCTOR INTEGRATED CIRCUIT
MOUNTING THE SAME



(57)Abstract:

PROBLEM TO BE SOLVED: To reliably protect a circuit of a structure that a plurality of circuits in which supply paths of a power supply power are independent in each circuit are combined to perform a desirable signal processing with the smaller number of protection elements from an extrinsic

abnormal high voltage.

SOLUTION: Out of a plurality of circuits A, B, C having at least pairs of power supply terminals and ground terminals (1A and 2A, 1B and 2B, 1C and 2C) which are independent for receiving a power supply power from external; and protection elements 6A, 6B, 6C between a power supply and a ground provided between the power supply terminal and the ground terminal, limiting to a combination of circuits (circuits A, B and circuits A, C) in which an interval between the circuits is connected by signal lines 9AB, 9AC, there are provided protection elements between the power supplies 7AB, 7CA and protection elements between the grounds 8AB, 8CA, between the power supply terminals (terminals 1A, 1B and terminals 1A, 1C), and between the ground terminals (terminals 2A, 2B and terminals 2A, 2C).

LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's
decision of rejection]

[Kind of final disposal of application
other than the examiner's decision of
rejection or application converted
registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's
decision of rejection]

[Date of requesting appeal against
examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

JPO and NCIPI are not responsible for any
damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1] The pair of the independent high order power supply terminal and lower order power supply terminal for receiving power from the exterior, As opposed to two or more circuits which have at least the high order and lower order power-sources protection component which an impedance falls and connects said high order power supply terminal and lower order power supply terminal by low impedance when it is prepared between said high order power supply terminals and lower order power supply terminals and the electrical potential difference beyond a predetermined value is added Among the high order power supply terminals between circuits, and among lower order power supply terminals, when the electrical potential difference beyond a predetermined value is added, an impedance falls. In the protection network in which the high order power-sources protection component which connects between said high order power supply terminals or between said lower order power supply terminals by low impedance, and the lower order power-sources protection component were prepared The protection network characterized by between circuits preparing said high order power-sources protection component and a lower order power-sources protection component only within the combination of the circuit to which it is connected with the signal line when there is combination of the circuit where

between circuits is not connected with a signal line to said two or more circuits.

[Claim 2] The circuit which at least one or more of the circuits connected with said signal line have an external terminal for exchanging the exterior and a signal, and has an external terminal for signal transfer with said exterior When the electrical potential difference beyond a predetermined value joins either [at least] between the external terminal for said signal transfer, and a high order power supply terminal, or between lower order power supply terminals, an impedance falls. The protection network according to claim 1 characterized by having the I/O protection component which connects between the external terminal for said signal transfer, and high order power supply terminals, or between lower order power supply terminals by low impedance.

[Claim 3] The pair of the independent high order power supply terminal and lower order power supply terminal for receiving power from the exterior on the same chip, Two or more circuits which have at least the high order and lower order power-sources protection component which an impedance falls and connects said high order power supply terminal and lower order power supply terminal by low impedance when it is prepared between said high order power supply terminals and lower order power supply terminals and the electrical potential difference beyond a predetermined value is added, When it is prepared among the high order power supply terminals between circuits, or among lower order power supply terminals and the electrical potential difference beyond a predetermined value is added, an impedance falls. In a semiconductor integrated circuit equipped with the high order power-sources protection component which connects between said high order power supply terminals or between said lower order power supply terminals by low impedance, and a lower order power-sources protection component The semiconductor integrated circuit characterized by between circuits preparing said high order power-sources protection component and a lower order power-sources protection component only within the combination of the circuit to which it is connected with the signal line when there is combination of the circuit where between circuits is not

connected with a signal line to said two or more circuits.

[Claim 4] The circuit which at least one or more of the circuits connected with said signal line have an external terminal for exchanging the exterior and a signal, and has an external terminal for signal transfer with said exterior When the electrical potential difference beyond a predetermined value joins either [at least] between the external terminal for said signal transfer, and a high order power supply terminal, or between lower order power supply terminals, an impedance falls. The semiconductor integrated circuit according to claim 3 characterized by having the I/O protection component which connects between said external terminals and high order power supply terminals or between lower order power supply terminals by low impedance.

[Claim 5] Claim 1 characterized by using pn junction diode for said high order and lower order power-sources protection component, a high order power-sources protection component, a lower order power-sources protection component, and an I/O protection component, a protection network according to claim 2, claim 3, or a semiconductor integrated circuit according to claim 4.

[Claim 6] Claim 1 characterized by using the metal oxide silicon field effect transistor which connected one side and the control electrode of a passage electrode to said high order and lower order power-sources protection component, the high order power-sources protection component, the lower order power-sources protection component, and the I/O protection component, and was considered as diode connection, a protection network according to claim 2, claim 3, or a semiconductor integrated circuit according to claim 4.

[Claim 7] At least 1 set in the combination of a circuit connected with said signal line is a semiconductor integrated circuit according to claim 3 to 6 characterized by the supply voltage of a mutual circuit differing.

[Translation done.]

* NOTICES *

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the circuit which protects the circuit of a configuration of performing desired signal processing about the semiconductor integrated circuit which carried a protection network and this combining two or more circuits with an independent power supply way especially different, respectively from a foreign abnormality high voltage like static electricity, and the semiconductor integrated circuit which carried such a protection network.

[0002]

[Description of the Prior Art] A semiconductor integrated circuit (LSI) is taken and explained to an example about this kind of protection network. Drawing 6 shows an example of arrangement of circuit Brock of LSI in which the protection network by the Prior art was carried. With reference to drawing 6 , this LSI is equipped with three circuits, Circuit A, Circuit B, and Circuit C, and Circuit A and Circuit B are connected with signal-line 9AB between circuits. Moreover, Circuit A and Circuit C are connected by signal-line 9AC between circuits. There is no signal line between circuits between Circuit B and Circuit C. Each circuits A, B, and C include an inverter, a NAND gate or the NOR gate of for example, a CMOS configuration, etc., respectively, and signal-line 9AB between Circuit A and Circuit B has connected the point (node of the drain electrodes of a pMOS transistor and a nMOS transistor) of Circuit A outputting [signal], and the signal

input point (common gate electrode of a pMOS transistor and a nMOS transistor) of Circuit B. The same is said of the combination of Circuit A and Circuit C.

[0003] In order to receive power independently from the exterior for every each, it equips each circuits A, B, and C with 1 set of group (1A, 2A and 1B, 2B, 1C and 2C) of an external power terminal and an external grand terminal at a time.

Moreover, in order to exchange the exterior and a signal, it has input/output terminals 3A, 3B, and 3C. Furthermore, Circuit A is equipped with I/O protection component 4A between power supply terminal 1A and input/output terminal 3A, it has I/O protection component 5A between grand terminal 2A and input/output terminal 3A, and a power source and glands protection component 6A are prepared between power supply terminal 1A and grand terminal 2A. Similarly, Circuit B is equipped with the protection components 4B, 5B, and 6B, and Circuit C has the protection components 4C, 5C, and 6C. Each protection component is for the abnormality high voltage preventing joining a circuit element like [in Circuit A (for example, the above-mentioned MOS transistor)] directly, and protecting a circuit, when it was the case of Circuit A and a foreign abnormality high voltage like static electricity is impressed to power supply terminal 1A which is an external terminal, grand terminal 2A, or input/output terminal 3A.

[0004] An above-mentioned I/O protection component, and a power source and a glands protection component It is the component which is in an insulating condition until a certain fixed electrical potential difference is built between terminals, and shows the property which will be in switch-on if the electrical potential difference beyond it is added. Fulfilling conditions, like time amount after that the electrical potential difference between terminals when changing to switch-on is the proof-pressure less or equal of the circuit element which should protect in Circuits A and B and C, the impedance at the time of a flow being low, and an electrical potential difference are impressed until it flows is short is called for. As a protection component, as long as it satisfies the above-mentioned conditions, may be the thing of what kind of structure, but if it is in a semiconductor integrated circuit The pn junction diode from a point, and the gate

electrode and drains () of a manufacture process, such as adjustment Or the forward voltage of an MOS transistor and the breakdown voltage of hard flow which tied the source electrode and were made diode connection are used in many cases. What is independent or used pn junction diode as shows several examples to drawing 7 , and the MOS transistor of diode connection as the protection component combining plurality is connected between the external power terminal of each circuits A, B, and C, an external I/O terminal, and an external grand terminal, as an example is shown in drawing 8 .

[0005] Although three circuits A, B, and C exchange a signal between the exterior or mutual circuits and perform desired signal processing as the whole LSI, LSI shown in this drawing 6 here If it says in connection with this invention, Circuit A and Circuit B will be connected with signal-line 9AB. Circuit A and Circuit C are connected with signal-line 9AC, and one description is between Circuit B and Circuit C to exchanging a signal mutually in a point without transfer of a signal, i.e., the point that all circuits are not connected with a signal line. Moreover, another description is in the point that each circuits A, B, and C are equipped with the group of the external power terminal for receiving supply of power from the exterior, and an external grand terminal mutually-independent. This invention is concerned with the technique which protects the circuit equipped with two above-mentioned descriptions from foreign abnormal voltage like static electricity.

[0006] The second above-mentioned description is based on the following reasons. That is, generally LSI is the circuit (it is hereafter described as a small circuit.) where the shoes formed on the same chip became independent. the circuits A, B, and C in drawing 6 -- corresponding -- it is connected with a signal line, and desired signal processing is performed, exchanging a signal between the exterior and a chip or among small circuits, and, naturally power required for actuation must be supplied to each smallness circuit. Supply of the power to this small circuit is realizable by preparing one pair of pair of the high order power supply terminal for receiving power from the exterior, and a lower order power

supply terminal on a chip most simply, and running a power-source line in all the small circuits on a chip from one pair of those external power terminals. However, LSI large-scale-izes and trouble arises [LSI] increasingly in the target signal processing in connection with advanced features and high-performance-izing in recent years with the structure which supplies power to all the small circuits on a chip only with one pair of above external power terminals.

[0007] When the power-source line is being carried out in common, it may be made the instability of each smallness circuit of operation, or fluctuation (the fall of high order power-source potential or rise of lower order power-source potential) of the supply voltage of the noise nature produced on the power-source line may make malfunction cause through a power-source line as an example depending on the case. Like [in order to exchange plurality, and an external circuit and an external signal, when the large circuits of the operating current like an output buffer carry out switching all at once], fluctuation of the supply voltage of the above-mentioned noise nature is produced, when the big operating current flows temporarily on a power-source line with actuation of each smallness circuit, the power-source potential VCC falls by wiring resistance of a power-source line or ground potential comes floating. if power shall be supplied to all the small circuits in LSI by every one high order power-source line and lower order power-source line each when such a phenomenon occurs for example, the power-source potential VCC and ground potential of another small circuit will also change a lot in some of some small circuits operating to coincidence -- things --

** Consequently, in the another small circuit, a margin of operation becomes small to the amplitude of the signal treated there, that it is easy to cause malfunction, it becomes, or the amplitude of an output signal becomes small, and the small circuit of the next step becomes easy to malfunction. Furthermore, depending on extent of a noise, the condition of a small circuit may be reversed only in a noise. Then, by making separate a high order power-source line and lower order power-source line in a certain small circuit and other small circuits, through a high order power-source line or a lower order power-source line, other

small circuits are made into instability of operation, or fluctuation of the supply voltage of the noise nature by a certain small circuit operating intercepts making it malfunction.

[0008] Again, with reference to drawing 6 , LSI shown in this drawing is equipped with I/O protection component 4A, 5A and 4B, and 5B, 4C and 5C for every circuits A, B, and C, and has a power source and the glands protection components 6A, 6B, and 6C. Therefore, even if an abnormality high voltage like static electricity is impressed between which external terminals the whole circuit, the charge by it discharges on the power-source line or grand line of each circuit through the protection component of each circuit, the great portion of energy of static electricity is consumed by the protection component, and the component inside a circuit is escaped from destruction. For example, in Circuit A, static electricity should be impressed between input/output terminal 3A and grand terminal 2A. In this case, the charge by static electricity flows to grand line 12A through I/O protection component 5A, and static electricity does not join the component in Circuit A. Similarly, Circuit A is protected when static electricity is added between input/output terminal 3A and power supply terminal 1A, and a charge flows to power-source line 11A through I/O protection component 4A. Moreover, Circuit A is protected by a power source and glands protection component 6A when static electricity is added between power supply terminal 1A and grand terminal 2A. Thus, Circuit A is protected by the protection components 4A, 5A, and 6A even if the foreign abnormality high voltage joins any of external power terminal 1A, external grand terminal 2A, or input/output terminal 3A to Circuit A. The same thing can say also about the circuit B of two others, and Circuit C.

[0009] However, when it thinks by the whole LSI, and the abnormality high voltage is added between the external terminals of circuit where the external terminal of a certain circuit and this are another, a protection feature does not act but a circuit may be destroyed. The explanation is given to below. The condition that static electricity joined drawing 8 between the external terminal of for

example, the circuit A and the external terminal of Circuit B is shown. In addition, in the following explanation, since especially the circuit C in this case does not participate in protected operation, drawing 8 excludes and shows the part of Circuit C, in order to make this simple and to make an understanding easy. With reference to drawing 8 , static electricity with which the direction of input/output terminal 3A serves as forward between input/output terminal 3A of Circuit A and grand terminal 2B of Circuit B should be added. At this time, as the continuous line as which the arrow head was attached in drawing 8 shows the charge by static electricity, it passes along I/O protection component 4A of Circuit A, and 1 ** flows to power-source line 11A of Circuit A. However, since the power-source line 11A is not connected to all wiring by the side of the point and Circuit B from it The charge which flowed to power-source line 11A flows backwards inside Circuit A, passes along component 10AB to signal-line 9AB which is in Circuit A and outputs a signal to Circuit B, passes along component 10BA which is in Circuit B and receives a signal from Circuit A further, and escapes from it to grand line 12B of Circuit B. Consequently, component 10AB and component 10BA which are in Circuit A and Circuit B, and exchange a signal through signal-line 9AB will be destroyed.

[0010] Destruction of the circuit which it produces that the supply way of power has been independent for every above circuits A, B, and C owing to can be prevented by inserting a protection component among the power-source lines between circuits, and among grand lines. The plot plan of circuit Brock of LSI of structure who prepared the protection component in drawing 9 between the power-source lines between each circuit and grand lines is shown. With reference to drawing 9 , as for LSI shown in this drawing, protection component 7AB, 7BC, and 7CA are connected [between power-source line 11A of Circuit A, and power-source line 11B of Circuit B] between power sources, respectively between power-source line 11B of Circuit B, and power-source line 11C of Circuit C, and between power-source line 11C of Circuit C, and power-source line 11A of Circuit A. Moreover, it has [between grand line 12A of Circuit A, and grand

line 12B of Circuit B] protection component 8AB, 8BC, and 8CA between glands, respectively between grand line 12B of Circuit B, and grand line 12C of Circuit C, and between grand line 12C of Circuit C, and grand line 12A of Circuit A. The thing of structure as shown in drawing 7 (b) is used for each of protection component 8AB, 8BC, and 8CA between power sources between protection component 7AB, 7BC, 7CA, and a gland. Many protection components of this structure are used when the supply voltage of both circuits is equal. Moreover, when one of supply voltage is low, the thing of the structure shown in drawing 7 (a) is used. Furthermore, although it is then rarely, when the voltage variation in the both ends of a protection component is large and flows also through a normal state with the structure of drawing 7 (a) and drawing 7 (b), the thing of the structure shown in drawing 7 (c) and drawing 7 (d) may be used.

[0011] make it any -- in LSI of the structure shown in drawing 9 , if static electricity with which the direction of input/output terminal 3A is just having mentioned above similarly between input/output terminal 3A of Circuit A and grand terminal 2B of Circuit B should be added The charge by this flows from I/O protection component 4A to power-source line 11A of Circuit A, as the continuous line as which the arrow head was attached in drawing 9 shows. Furthermore, it passes along protection component 7AB between the power sources established between the power-source line of Circuit A, and the power-source line of Circuit B, and escapes from the power source and glands protection component 6B of Circuit B to grand line 12B. Or as the broken line to which the arrow head was attached shows, it flows from I/O protection component 5A to grand line 12A of Circuit A, it passes along protection component 8AB further between the glands prepared between the grand line of Circuit A, and the grand line of Circuit B, and escapes to grand line 12B of Circuit B. It is decided along which discharge path it will pass by the electrical potential difference from which a protection component, and the impedance or protection component of wiring changes to switch-on. Although it is the example in which the abnormality high voltage was added between input/output terminal 3A of

Circuit A, and grand terminal 2B of Circuit B, having stated above Between three circuits A and B and C, even when the high voltage is added between each external terminals 1A, 2A, 3A, and 1B, 2B, and which combination of 3B, 1C, 2C, and 3C Moreover, even when which discharge path is followed, the charge by static electricity does not flow into the interior of Circuit A and Circuit B, and each circuits A, B, and C are protected certainly.

[0012]

[Problem(s) to be Solved by the Invention] As are mentioned above and it is shown in drawing 9 , also in the case of LSI of the structure where each smallness circuit on a chip receives supply of power independently of the exterior for every each, among each smallness circuits Even when the foreign abnormality high voltage is impressed between the external terminals of a different small circuit by preparing a power-sources protection component or a glands protection component, respectively between a power-source line and a power-source line and between a grand line and a grand line, each smallness circuit can be protected from destruction.

[0013] However, if a power-sources protection component and a glands protection component are prepared to the combination of all small circuits and the number of small circuits and the number of the supply ways of the power which became independent when putting in another way will increase as shown in drawing 9 , the problem that the number of a power-sources protection component and glands protection components will increase very much along with it will arise. That is, if the number of small circuits is made into n pieces (2 or more [However, n]), it is the number of the groups of a power-sources protection component and a glands protection component. Become the number expressed with $nC2 = n(n-1) / 2$, and if the number of small circuits is three Although it ends with 3 sets as the group of a protection component is shown in drawing 9 , if the five numbers of small circuits become and 10 sets will become six pieces, the number of the groups of a power-sources protection component and a glands protection component will increase in the condition of 15 sets

rapidly with the increment in the number of small circuits, and will be carried out to it.

[0014] Therefore, this invention aims at being a small number of protection components and enabling it to protect certainly the circuit of a configuration of performing desired signal processing combining two or more circuits which made the supply way of power become independent for every circuit from the foreign abnormality high voltage.

[0015]

[Means for Solving the Problem] The pair of the independent high order power supply terminal and a lower order power supply terminal for the protection network of this invention to receive power from the exterior, As opposed to two or more circuits which have at least the high order and lower order power-sources protection component which an impedance falls and connects said high order power supply terminal and lower order power supply terminal by low impedance when it is prepared between said high order power supply terminals and lower order power supply terminals and the electrical potential difference beyond a predetermined value is added Among the high order power supply terminals between circuits, and among lower order power supply terminals, when the electrical potential difference beyond a predetermined value is added, an impedance falls. In the protection network in which the high order power-sources protection component which connects between said high order power supply terminals or between said lower order power supply terminals by low impedance, and the lower order power-sources protection component were prepared When there is combination of the circuit where between circuits is not connected with a signal line to said two or more circuits, it is characterized by between circuits preparing said high order power-sources protection component and a lower order power-sources protection component only within the combination of the circuit to which it is connected with the signal line.

[0016] Moreover, the pair of the independent high order power supply terminal and a lower order power supply terminal for the semiconductor integrated circuit

of this invention to receive power from the exterior on the same chip, Two or more circuits which have at least the high order and lower order power-sources protection component which an impedance falls and connects said high order power supply terminal and lower order power supply terminal by low impedance when it is prepared between said high order power supply terminals and lower order power supply terminals and the electrical potential difference beyond a predetermined value is added, When it is prepared among the high order power supply terminals between circuits, or among lower order power supply terminals and the electrical potential difference beyond a predetermined value is added, an impedance falls. In a semiconductor integrated circuit equipped with the high order power-sources protection component which connects between said high order power supply terminals or between said lower order power supply terminals by low impedance, and a lower order power-sources protection component When there is combination of the circuit where between circuits is not connected with a signal line to said two or more circuits, it is characterized by between circuits preparing said high order power-sources protection component and a lower order power-sources protection component only within the combination of the circuit to which it is connected with the signal line.

[0017]

[Embodiment of the Invention] Next, the gestalt of operation of this invention is explained with reference to a drawing. Drawing 1 is drawing showing an example of arrangement of circuit Brock of the semiconductor integrated circuit concerning the gestalt of 1 operation of this invention. If drawing 1 is compared with drawing 9 , LSI concerning the gestalt of this operation The point of having prepared the power-sources protection component between power-source line 11A of Circuit A, and power-source line 11B of Circuit B, and only within between power-source line 11A of Circuit A, and power-source line 11C of Circuit C, It differs from LSI by the Prior art in that the glands protection component is connected only between grand line 12A of Circuit A, and grand line 12B of Circuit B, and between grand line 12A of Circuit A, and grand line 12C of Circuit C. That is, LSI

shown in drawing 1 will be prepared only among the circuits (Circuit A, Circuit B, and Circuit A and a circuit (C)) by which the power-sources protection component and the glands protection component are connected with the signal line.

[0018] Circuit Brock's plot plan of the 1st example which used pn junction diode for drawing 2 at the I/O protection component, the power-sources protection component, and the glands protection component is shown. Moreover, in LSI shown in drawing 2 , a condition when static electricity with which the direction of input/output terminal 3A serves as forward between input/output terminal 3A of Circuit A and grand terminal 2B of Circuit B is added is shown in drawing 3 . In addition, in the following explanation, since especially the circuit C in this case does not participate in protected operation, drawing 3 excludes and shows the part of Circuit C, in order to make this simple and to make an understanding easy. As the continuous line which put the arrow head in drawing 3 shows, the charge by static electricity impressed to input/output terminal 3A of Circuit A flows from I/O protection component 5A to grand line 12A by the side of the grand line of Circuit A, passes along protection component 8AB further between the glands prepared between the grand line of Circuit A, and the grand line of Circuit B, and escapes from it to the grand line 12B of Circuit B with reference to drawing 3 . Or as the broken line to which the arrow head was attached shows, it flows from I/O protection component 4A to power-source line 11A by the side of the power-source line of Circuit A, it passes along protection component 7AB further between the power sources established between the power-source line of Circuit A, and the power-source line of Circuit B, and escapes from the power source and glands protection component 6B of Circuit B to grand line 12B. Although it is decided along what kind of discharge path it will pass by the electrical potential difference from which a protection component, and the impedance or protection component of wiring changes to switch-on, since the charge by static electricity flows protection component 8AB between protection component 7AB or a gland between the power sources between circuits and it does not flow into the interior of Circuit A and Circuit B even when which discharge path is followed, Circuits A

and B are both protected certainly.

[0019] Next, the condition that static electricity with which the direction of input/output terminal 3C serves as forward between input/output terminal 3B of Circuit B and input/output terminal 3C of Circuit C joined drawing 4 as other examples in case static electricity is added is shown. With reference to drawing 4 , the charge by static electricity impressed to input/output terminal 3C of Circuit C in this case As the continuous line as which the arrow head was attached in drawing 4 shows, it flows to power-source line 11C through I/O protection component 4C of Circuit C, and flows to power-source line 11A further through power-sources protection component 7CA prepared between power-source line 11C of Circuit C, and power-source line 11A of Circuit A. Subsequently, it passes along power-sources protection component 7BA prepared between power-source line 11A of Circuit A, and power-source line 11B of Circuit C, flows to power-source line 11B of Circuit B, finally it passes along I/O protection component 4B of Circuit B, and flows to input/output terminal 3B of Circuit C. Or as the broken line to which the arrow head was attached shows Between the glands between grand line 12C of I/O protection component 5C-> grand line 12C-> circuit C of Circuit C, and grand line 12A of Circuit A, grand line 12A of the protection component 8CA-> grand line 12A-> circuit A It flows in the path of input/output terminal 3B of the I/O protection component 5B-> circuit C of the grand line 12B-> circuit B of the glands protection component 8AB-> circuit B between grand line 12B of Circuit B. Even when it passes along which discharge path, the charge by static electricity does not flow into the interior of Circuit A and Circuit B, and each circuits A, B, and C are protected certainly.

[0020] As already stated, it is LSI which made the power supply terminal and the grand terminal become independent for every circuit, and changed the power supply way, and the place which is easy to be destroyed especially with static electricity is a circuit element linked to the signal line to which between each circuit is connected. If this is in LSI of the structure where no protection components are inserted among the power supply terminals between circuits as

shown in drawing 6 , and among grand terminals Static electricity which joined the external terminal for every circuit in it is alike and straddling the circuit where static electricity differs, although the power-source line or grand line of a circuit distributes and the component in each circuit is not destroyed It is because the circuit element which the charge by the static electricity will flow from one circuit to the circuit of another side through the signal line between circuits, and connects to the signal line as a result is destroyed.

[0021] On the other hand, by inserting a protection component among each circuits A, B, and C between the power-source lines of the circuits connected with the signal line, and between grand lines according to this invention Since static electricity impressed from the outside of LSI flows through protection component 8AB between protection component 7AB(s), 7CAs, and the grand lines between power-source lines, and 8CA even when crossing among the external terminals of a different circuit Each circuits A, B, and C are not destroyed by static electricity through the interior of Circuit A, Circuit B, or Circuit C.

[0022] And since he is trying to prepare the power-sources protection component between different circuits, and a glands protection component only within between the circuits mutually connected with the signal line in the case of this invention, the group of a power-sources protection component and a grand protection component will require only the number of the signal lines to which each circuit in a chip is connected. Usually, since it is rare to connect all small circuits with the signal line and each smallness circuit is connected to a serial according to the processing path of a signal in many cases even when making a still bigger circuit combining some circuits, when the most, the group of a power-sources protection component and a glands protection component can be managed with number extent of a small circuit. For example, the group of a power-sources protection component in case all small circuits are completely connected to the serial like the circuits A, B, C, and D in the 2nd example which shows circuit Brock's plot plan to drawing 5 , and a glands protection component

can be managed with a group (several [of a small circuit] -1).

[0023] In addition, in the gestalt of this operation, although each circuit A, B, and C shall be altogether equipped with the input/output terminals (exterior) 3A, 3B, and 3C for exchanging the exterior and a signal, even if all circuits do not necessarily have the input/output terminal connected outside, the operation effectiveness of this invention is not spoiled. Moreover, although the gestalt of this operation explained the example using the input/output terminal of structure changed and used for the object for an input, and an output with one terminal as external terminals 3A, 3B, and 3C close and for the output of a signal, this terminal may be the terminal of an input only, or a terminal of an output only. When it does not have the input/output terminal, input terminal, or output terminal as an external terminal, it is necessary not to dare prepare an I/O protection component in each circuits A, B, C, and D like LSI of the 2nd example shown in drawing 5 .

[0024] Moreover, in the 1st example shown in drawing 2 , between power sources, between protection component 7AB, 7BC, 7CA, and a gland, although the example which used the thing of the same structure for protection component 8AB, 8BC, and 8CA altogether was shown, this invention is not restricted to this. Although the digital circuit and the analog circuit were made intermingled, there are some from which supply voltage differs in each circuits [like] A, B, and C in LSI. When such, from some protection components shown in drawing 7 as a power-sources protection component or a glands protection component according to the supply voltage of each circuits A, B, and C, that from which structure differs can be chosen suitably and can be combined. In drawing 1 , the supply voltage of Circuit B is the same as the supply voltage of Circuit A. For example, when the supply voltage of Circuit C is higher than it The thing of the structure shown in drawing 7 (b) is used for protection component 8AB between protection component 7AB and a gland between the power sources between Circuits A and B. What is necessary is to make the anode of diode into Circuit A side, and just to make a cathode into Circuit C side using the protection

component of the structure shown in power-sources protection component 7CA between Circuits A and C, and glands protection component 8CA at drawing 7 (a). It does not matter even if it uses the thing of structure different, respectively from the relation of the amplitude of an I/O signal similarly about the input/output terminal protection components 4A, 5A, 4B, 5B, 4C, and 5C.

[0025] furthermore, a power source and the glands protection components 6A, 6B, and 6C prepare -- having -- **** -- if it carries out, the protection components 5A, 5B, and 5C between the protection components 4A, 4B, and 4C between a power supply terminal and an input/output terminal, a grand terminal, and an input/output terminal will not necessarily become a pair -- **** -- either -- it does not matter. When either one of the two is excluded, it is desirable to double the current capacity of remaining one of the two's protection component so that the impedance when flowing may become sufficiently low. Moreover, it is not necessary to also necessarily prepare protection component 7AB, glands protection component 8AB, power-sources protection component 7CA, and glands protection component 8CA by the pair between power sources, and only either is. However, it be necessary to enlarge current capacity in the direction of the remainder, and probably, it will be desirable, as mention above, when make it only either for an I/O protection component to also prepare a power sources protection component and a glands protection component by the pair like the gestalt of this operation from a viewpoint of secure the versatility of a discharge path, practically, since there be few advantages on the monopoly area of a protection component.

[0026] In addition, although the semiconductor integrated circuit was made into the example and explained until now, again In the circuit of a configuration of performing desired signal processing with the combination of two or more small circuits The phenomenon in which fluctuation of the supply voltage of the noise nature accompanying actuation of a certain small circuit has a bad influence on the condition of other small circuits, or actuation through a common power-source line, About the cure of intercepting, that fluctuation of supply voltage

spreads by making the supply way of power become independent for every settlement of every small circuit and some small circuits If "LSI" is read as an "electronic instrument" and a "chip" is read as a "case", generally it will be clear that this invention is applicable also to an electronic instrument.

[0027]

[Effect of the Invention] As explained above, according to this invention, the circuit of a configuration of performing desired signal processing combining two or more circuits which made the supply way of power become independent for every circuit can be certainly protected from the foreign abnormality high voltage with few protection components of a number.

[Translation done.]

* NOTICES *

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is drawing showing an example of arrangement of circuit Brock of the semiconductor integrated circuit concerning the gestalt of 1 operation of this invention.

[Drawing 2] It is drawing showing arrangement of circuit Brock of LSI concerning the 1st example.

[Drawing 3] In the 1st example, it is drawing showing a condition when static electricity is added between the input/output terminal of Circuit A, and the grand terminal of Circuit B.

[Drawing 4] In the 1st example, it is drawing showing a condition when static electricity is added between the input/output terminal of Circuit C, and the input/output terminal of Circuit B.

[Drawing 5] It is drawing showing circuit Brock's plot plan of LSI concerning the 2nd example.

[Drawing 6] It is drawing showing arrangement of circuit Brock of LSI of an example by the Prior art.

[Drawing 7] It is drawing showing some examples of the structure of a protection component.

[Drawing 8] In LSI shown in drawing 6 , it is drawing showing a condition when static electricity is added between the input/output terminal of Circuit A, and the grand terminal of Circuit B.

[Drawing 9] It is drawing showing a condition when static electricity is added between arrangement of circuit Brock of LSI of other examples by the Prior art, and the input/output terminal of Circuit A and the grand terminal of Circuit B.

[Description of Notations]

1A, 1B, 1C Power supply terminal

2A, 2B, 2C Grand terminal

3A, 3B, 3C Input/output terminal

4A, 4B, 4C I/O protection component

5A, 5B, 5C I/O protection component

6A, 6B, 6C A power source and glands protection component

7AB(s), 7BC, 7CA Power-sources protection component

8AB(s), 8BC, 8CA Glands protection component

9AB(s), 9AC Signal line

11A, 11B, 11C Power-source line

12A, 12B, 12C Grand line

[Translation done.]

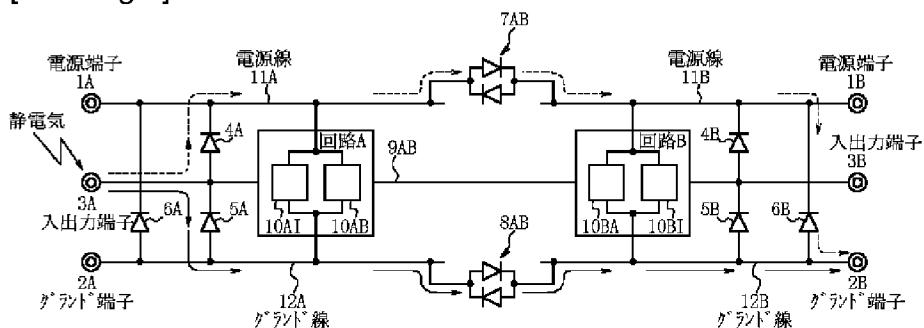
* NOTICES *

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

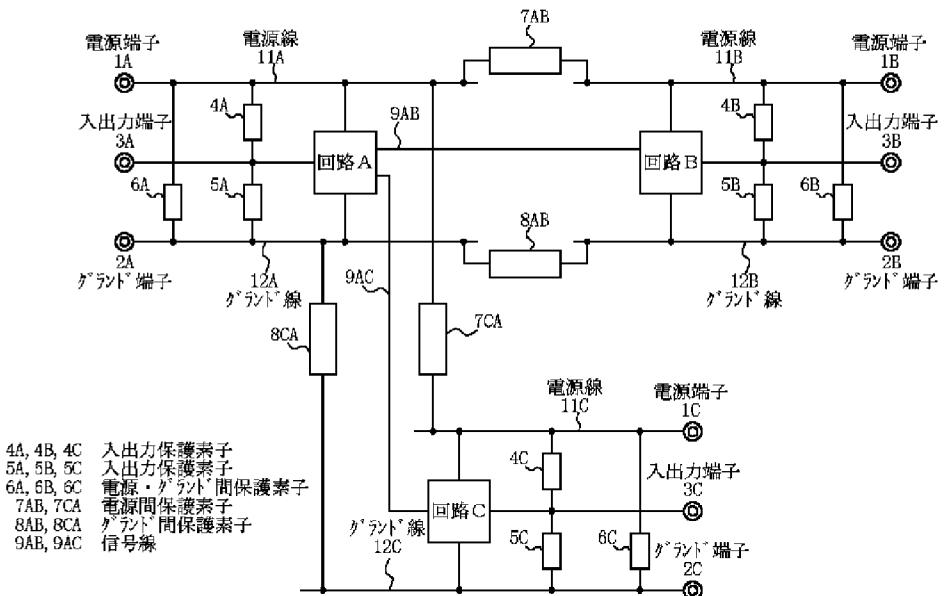
DRAWINGS

[Drawing 3]

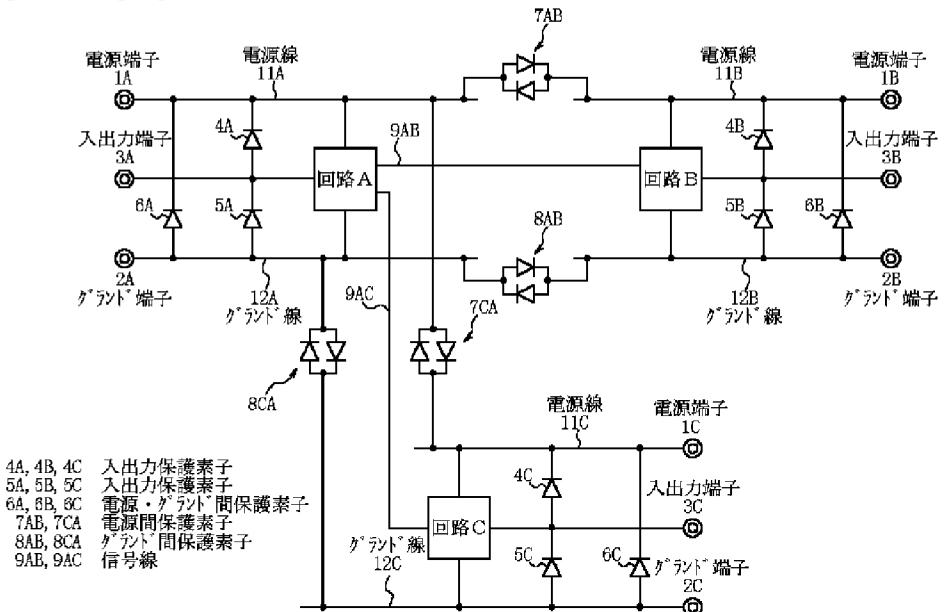


4A, 4B 入出力保護素子
5A, 5B 入出力保護素子
6A, 6B 電源・グランド間保護素子
7AB 電源間保護素子
8AB グランド間保護素子
9AB 信号線

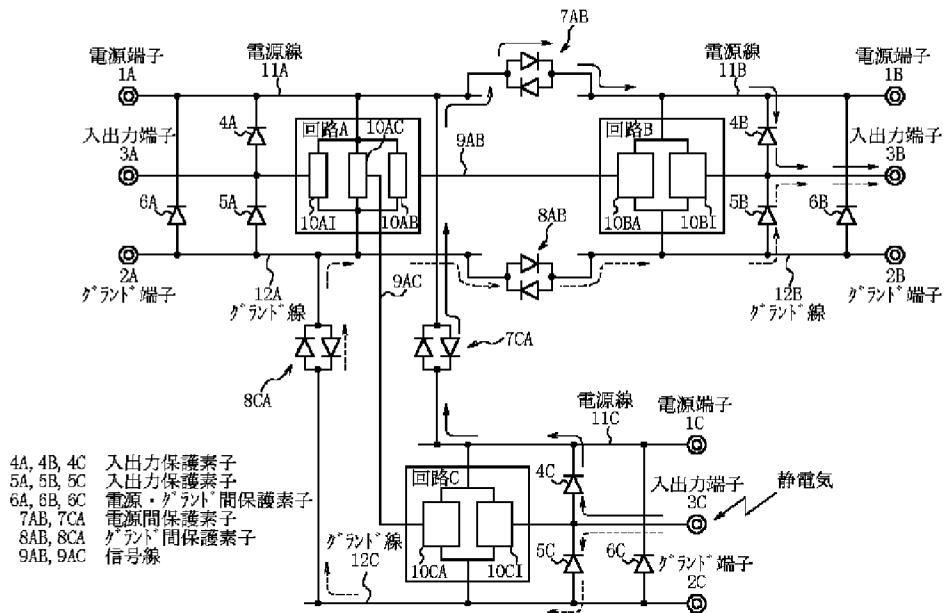
[Drawing 1]



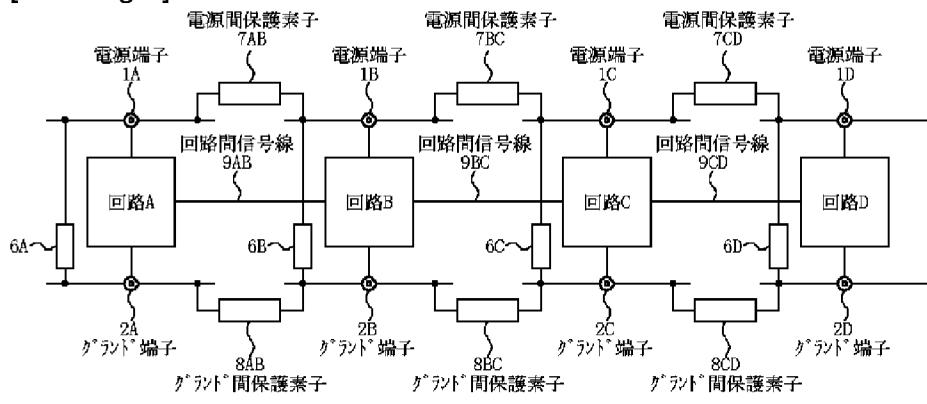
[Drawing 2]



[Drawing 4]

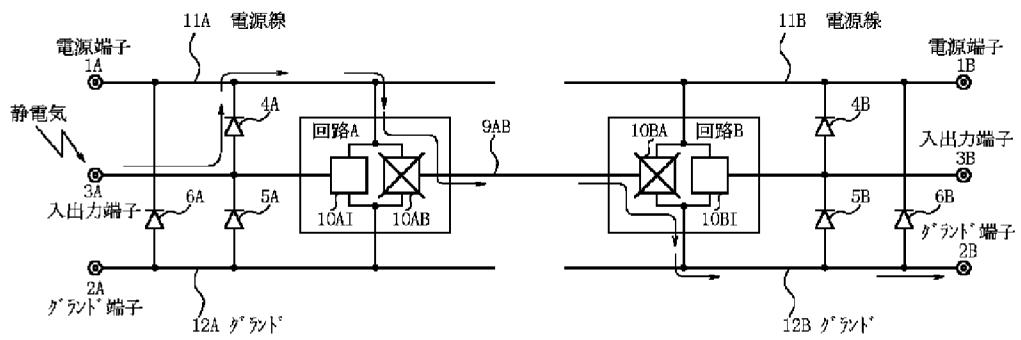


[Drawing 5]

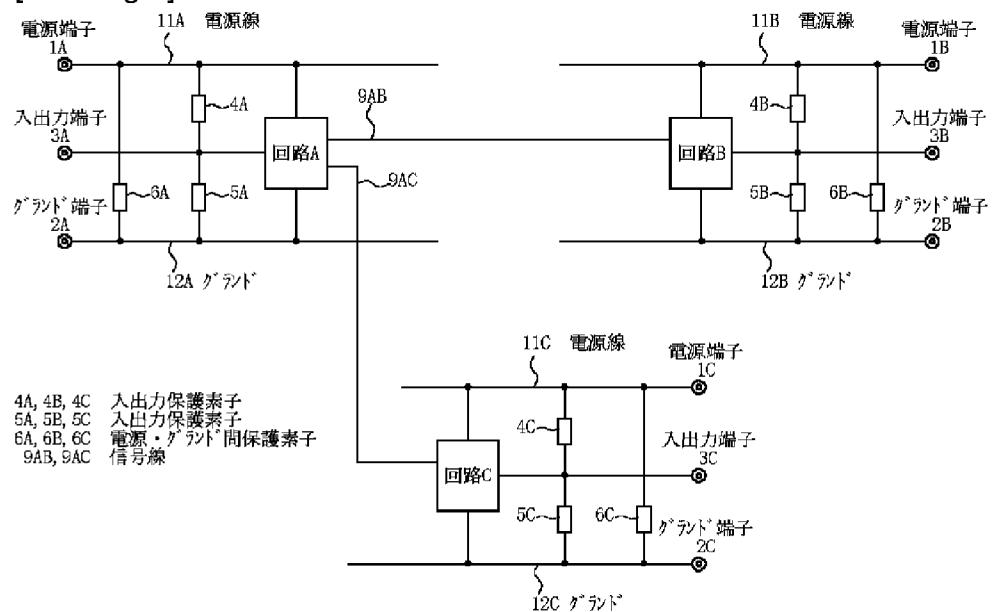


6A, 6B, 6C, 6D 電源・グランド間保護素子

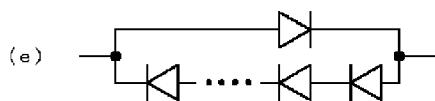
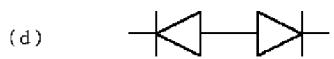
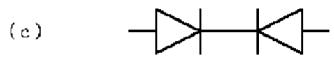
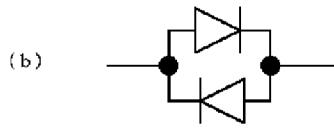
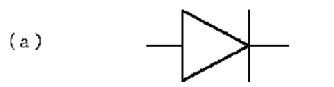
[Drawing 8]



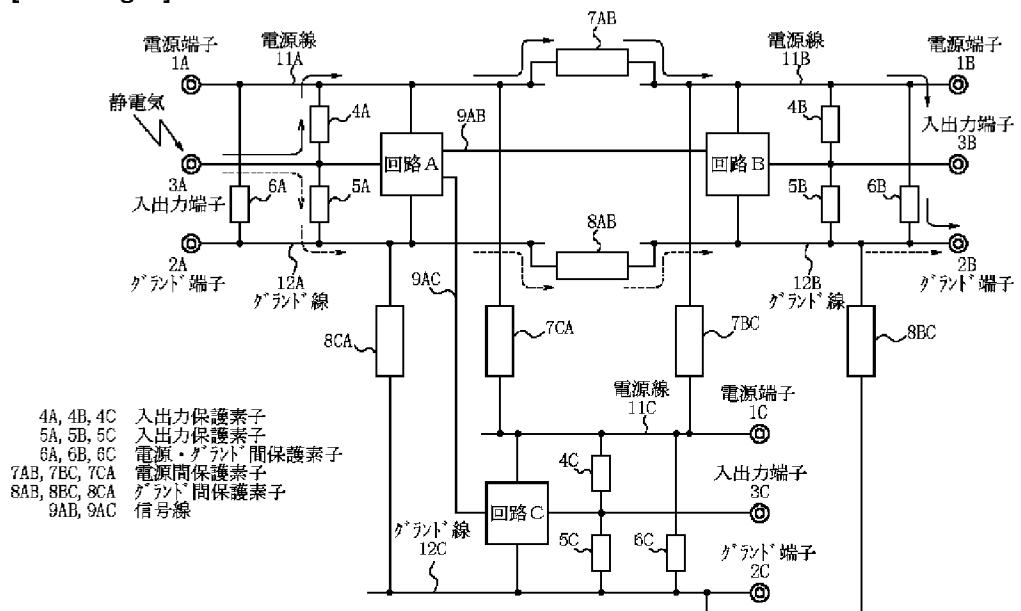
[Drawing 6]



[Drawing 7]



[Drawing 9]



[Translation done.]